Customer No.: 31561
Docket No.: 10607-US-PA
Application No.: 10/604,840

In the Claims

Please amend the claims as follows.

1. (currently amended) An operation method of a phase lock loop circuit, comprising:

obtaining a first value and a second value by a counter and respectively counting an input signal with a first frequency ~~received by the phase lock loop circuit within one cycle period~~ and ~~counting~~ an output signal with a second frequency from a voltage control oscillator within ~~the same~~ a cycle period;

obtaining a third value by comparing the difference of the first value and the second value and forwarding the third value to the voltage control oscillator; and

modifying the second frequency of the output signal as a modified output signal in response to the third value ~~for the phase lock loop circuit~~ and forwarding the modified output signal to [[a]] said counter ~~until the difference of the first value and the second value is substantial zero~~.

2. (currently amended) The operation method of a phase lock loop circuit as claimed in claim 1, wherein the speed of modifying the second frequency of the output signal of the voltage control oscillator varies with the third value~~, wherein when the third value becomes larger, the speed of modifying the second frequency of the output signal becomes faster, when the third value becomes smaller, the speed of modifying the second frequency of the output signal becomes slower~~.

3. (currently amended) The operation method of a phase lock loop circuit as claimed in claim 1, further comprising a step of dividing the first frequency of the input signal and obtaining the first value by counting the input signal with a divided first frequency. ~~wherein before obtaining the first value, the first frequency of the input signal received by the phase lock loop circuit is further divided by a first frequency divider with a first number and the first value is obtained in response to the divided first frequency of the input signal.~~

4. (original) The operation method of a phase lock loop circuit as claimed in claim 3, wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is further divided by a second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.

5. (currently amended) The operation method of a phase lock loop circuit as claimed in claim 1, further comprising a step of dividing the second frequency of the output signal and obtaining the second value by counting the output signal with a divided second frequency. ~~wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is further divided by a second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.~~

6. (currently amended) The operation method of a phase lock loop circuit as claimed in claim 1, further comprising a step of filtering the third value to filter out a high frequency

noise existed in the third value. ~~wherein before modifying the second frequency of the output signal in response to the third value, the third value is further filtered by a loop filter to filter out a high frequency noise existed in the phase lock loop circuit.~~

7. (original) The operation method of a phase lock loop circuit as claimed in claim 1, wherein the input signal with the first frequency is generated by a crystal oscillator.

8. (currently amended) The operation method of a phase lock loop circuit as claimed in claim 3 [[~~1~~]], wherein ~~combination of~~ the step of ~~calculating~~ counting the first frequency of the input signal ~~received by the phase lock loop circuit~~ and the step of dividing the first frequency of the input signal are performed by a programmable counter.

9. (currently amended) A phase lock loop circuit, comprising:

a counter, for obtaining a first value and a second value by respectively counting an input signal with a first frequency ~~received by the phase lock loop circuit within one cycle period~~ and counting an output signal with a second frequency within ~~the same~~ a cycle period, ~~wherein~~ and obtaining a third value ~~is obtained~~ by comparing [[~~the~~]] a difference of the first value and the second value; and

a voltage control oscillator for generating the output signal~~, wherein when the voltage control oscillator obtains the third value from the counter,~~ and modifying the frequency of the output signal in response to the third value ~~for the phase lock loop circuit~~.

10. (currently amended) The phase lock loop circuit as claimed in claim 9, wherein the speed of modifying the second frequency of the output signal of the voltage control oscillator

varies with the third value~~, wherein when the third value becomes larger, the speed of modifying the second frequency of the output signal becomes faster, when the third value becomes smaller, the speed of modifying the second frequency of the output signal becomes slower~~.

11. (currently amended) The phase lock loop circuit as claimed in claim 9, further comprising a first frequency divider, wherein ~~before obtaining the first value,~~ the first frequency of the input signal ~~received by the phase lock loop circuit~~ is further divided by the first frequency divider ~~with a first number~~ and the first value is obtained ~~in response to the divided first frequency of~~ by counting the input signal with a divided first frequency.

12. (original) The phase lock loop circuit as claimed in claim 11, further comprising a second frequency divider, wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is further divided by the second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.

13. (currently amended) The phase lock loop circuit as claimed in claim 9, further comprising a second frequency divider, wherein ~~before obtaining the second value,~~ the second frequency of the output signal from the voltage control oscillator is further divided by a second frequency divider ~~with a second number~~ and the second value is obtained ~~in response to the divided second frequency of~~ by counting the output signal with a divided second frequency.

14. (currently amended) The phase lock loop circuit as claimed in claim 9, further comprising a loop filter, ~~located~~ coupled between the counter and the voltage control oscillator for filtering the third value to filter out a high frequency noise existed in the third value., ~~wherein before modifying the second frequency of the output signal in response to the third value, the third value is further filtered by the loop filter to filter out a high frequency noise existed in the phase lock loop circuit.~~

15. (original) The phase lock loop circuit as claimed in claim 9, wherein the input signal with the first frequency is generated by a crystal oscillator.

16. (currently amended) The phase lock loop circuit as claimed in claim 11 [[9]], wherein the counter and a first frequency divider are combined together to form a programmable counter for generating various frequencies.